

WHAT IS CLAIMED IS:

Sub
A2 }
1. A nonvolatile semiconductor memory device comprising:

a semiconductor substrate;

5 a first transistor formed in a peripheral circuit portion of the semiconductor substrate, a gate electrode of the first transistor having a first gate length;

0055677 045500
10 a second transistor formed in a memory cell portion of the semiconductor substrate, a gate electrode of the second transistor having a second gate length shorter than the first gate length; and

15 a first insulating film formed above at least the memory cell portion, the first insulating film covering the second transistor and having a property which makes it difficult for an oxidizing agent to pass therethrough.

20 2. The nonvolatile semiconductor memory device according to claim 1, wherein the gate electrode of the second transistor has a stacked gate structure which includes a floating gate formed on a gate insulating film, an inter-gate insulating film formed on the floating gate and a control gate formed on the inter-gate insulating film.

25 3. The nonvolatile semiconductor memory device according to claim 1, further comprising:

a second insulating film which is different from

Sub A2 >

the first ~~C~~ insulating film and formed between at least the second transistors and the first insulating film.

4. ~~A~~ The nonvolatile semiconductor memory device according to claim 1, wherein the first insulating film is used as an etching stopper when contact holes are formed.

5. The nonvolatile semiconductor memory device according to claim 1, wherein the surfaces of the gate electrodes of the first and second transistors are oxidized.

6. A method for manufacturing a nonvolatile semiconductor memory device comprising:

forming a first gate electrode, which has a first gate length, on a peripheral circuit portion of a semiconductor substrate and a second gate electrode, which has a second gate length shorter than the first gate length, on a memory cell portion of the semiconductor substrate;

introducing impurity into the peripheral circuit portion and memory cell portion with at least the first and second gate electrodes used as a mask;

forming a first insulating film above at least the memory cell portion, the first insulating film covering the second transistors and having a property which makes it difficult for an oxidizing agent to pass therethrough; and

annealing the semiconductor substrate into which

005240" 2295560

the impurity has been introduced in an oxidation atmosphere to diffuse the impurity into the semiconductor substrate, whereby a first transistor having the first gate electrode and source and drain diffusion layers containing the diffused impurity is formed in the peripheral circuit portion and a second transistor having the second gate electrode and source and drain diffusion layers containing the diffused impurity is formed in the memory cell portion.

7. The method for manufacturing the nonvolatile semiconductor memory device according to claim 6, wherein at least the second gate electrode is formed by a method including steps of forming a gate insulating film on the semiconductor substrate, forming a floating gate on the gate insulating film, forming an inter-gate insulating film on the floating gate and forming a control gate on the inter-gate insulating film.

8. The method for manufacturing the nonvolatile semiconductor memory device according to claim 6, further comprising:

forming a second insulating film which is different from the first insulating film and formed between at least the second transistors and the first insulating film.

9. The method for manufacturing the nonvolatile semiconductor memory device according to claim 6, further comprising:

forming an inter-level insulating film above the semiconductor substrate after annealing the semiconductor substrate;

5 forming a first contact hole reaching the first insulating film in the inter-level insulating film; and

etching a part of the first insulating film which are exposed to the bottoms of the first contact hole and forming a second contact hole reaching a source/drain diffusion region of the second transistor in the first insulating film.

10 10. The method for manufacturing the nonvolatile semiconductor memory device according to claim 6, further comprising;

15 subjecting the surfaces of the first and second gate electrodes to an oxidation process.

11. A nonvolatile semiconductor memory device comprising:

a semiconductor substrate;

20 a transistor formed in a memory cell portion of the semiconductor substrate; and

a silicon nitride film whose surface is oxidized, the silicon nitride film covers the transistor.

12. The nonvolatile semiconductor memory device according to claim 11, wherein the silicon nitride film has a thickness of at most 50 nm.

13. The nonvolatile semiconductor memory device according to claim 11, wherein the thickness of an

00556777-042500

SUBA3

Sub
A3

oxide film on the surface of the silicon nitride film is not smaller than 1 nm and not larger than 10 nm.

14. The nonvolatile semiconductor memory device according to claim 11, wherein the concentration of hydrogen in the silicon nitride film is not larger than 3×10^{21} atom/cm³.

15. A method for manufacturing a nonvolatile semiconductor memory device:

forming a transistor in a memory cell portion of a semiconductor substrate;

covering the transistor with a silicon nitride film; and

subjecting the surface of the silicon nitride film to an oxidation process.

16. The method for manufacturing the nonvolatile semiconductor memory device according to claim 15, further comprising:

forming an inter-level insulating film on the semiconductor substrate after subjecting the surface of the silicon nitride film to an oxidation process.

17. The method for manufacturing the nonvolatile semiconductor memory device, according to claim 15, wherein the surface of the silicon nitride film is oxidized by a method selected from the group consisting of pyrogenic oxidation and water-vapor oxygen oxidation.

18. The method for manufacturing the nonvolatile semiconductor memory device, according to claim 16,

wherein the surface of the silicon nitride film is oxidized by a method selected from the group consisting of pyrogenic oxidation and water-vapor oxygen oxidation.

ALL A4 >

005240-2295550